This application is a continuation of and claims priority to U.S. Patent Application having an application number 10/218,348, filed 08/14/2002, now Patent No. 6,674,671 which application is hereby incorporated by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention is related to the field of circuits for handling multiple possible drivers of a line.

2. Description of the Related Art

In circuit design, there are many uses for a line (or buses comprising multiple lines) which may have multiple drivers of the line. Generally, one of the drivers may drive the line at any given time. For example, memory arrays such as caches may employ such a structure for each bit read from the memory array. The memory array may include multiple banks, one of which may be read at any given time. Each bank has an output that may drive the line corresponding to the bit, and the bank that is being read drives the line. As another example, communication lines between two or more circuits may be driven by any of the circuits according to some protocol (often referred to as bi-directional lines, since the lines may be inputs or outputs of a given circuit at a given point in time).

Fig. 1 illustrates a first prior art circuit providing for multiple drivers of a line (the line is illustrated as carrying a D_{out} signal in Fig. 1, and may be referred to herein as the D_{out} line). The circuit of Fig. 1 may sometimes be referred to as a low swing, dual rail dynamic circuit. Each driver may drive a dynamic data signal and its complement (e.g. the dynamic data signal d0 and its complement d0# may be driven by a first driver and the dynamic data signal d1 and its complement d1# may be driven by a second driver). In